**INTRODUCCION**

The uninterrupted and progressive miniaturization of microelectronic devices while resulting in more powerful computers, has also made these computers more susceptible to the effects of ionizing radiation.

La ininterrumpida y progresiva disminución en tamaño de los dispositivos micro-electrónicos, mientras genera como resultado computadores cada vez más potentes, también ocasiona que estos sean cada vez más susceptibles a efectos de ionización por radiación.

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The constant evolution of technologies which are employed to manufacture integrated

circuits has lead to a drastic reduction of transistor dimensions. This

process converges to a limit at which an invulnerability to errors, caused by

external agents is very unlikely. These faults reduce the reliability of the considered

circuits.

Esta constante evolución de la tecnología impulsada por las grandes compañías manufacturadoras de circuitos integrados a llevado a la dramática reducción en el dimensionamiento de los transistores. Dicho proceso converge hasta un límite en el cual la invulnerabilidad a errores causados por agentes externos es muy poco deseada, reduciendo la fiabilidad de los circuitos considerados.

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**Single Event Phenomena**

Microelectronic devices are susceptible to damage or interruption from exposure to radiation. Such devices contain structures made up of semiconductor materials that operate by regulating current flow or the amount of electrical charge held in a potential well. Interaction with radiation, including any energetic particle (electrons, protons, neutrons) or photon (gamma rays, X-rays), alters these precisely regulated conditions and produces SEP (see sidebar, [Types of Single Event Effects](http://www.aero.org/publications/crosslink/winter2000/03_sidebar1.html)).

Los dispositivos micro electrónicos son susceptibles a danos o interrupciones al ser expuestos a la radiación debido a su estructura y forma de funcionamiento. Dicha estructura está hecha de material semiconductor que opera por regulaciones de flujo de corriente o por la cantidad de carga eléctrica acumulada en un pozo de potencial (potential well). La interaccion con radiación, incluyendo cualquier particula energética (electronces, protones, neutrones) o fotones (rayos gamma, rayos X) altera estas condiciones precisas de regulación y se producen SEPs (Single Event Phenomena)

SEP are classified by the type of effect that occurs in the device, known as a single event effect (SEE). Types of SEE include single event upset (SEU), latchup, burnout, gate rupture, and total dose.

SEP son clasificados por el tipo de efecto que ocurre en el dispositivo, conocidos como Single Event Effect (SEE).

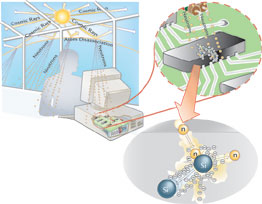
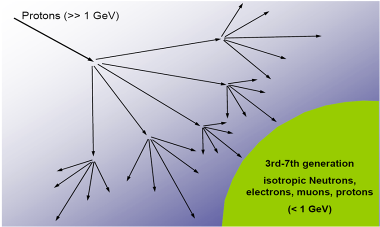
**HISTORIA**

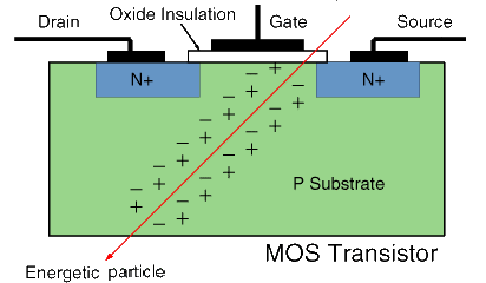
Several years after single event upset (SEU) was discovered in space in 1975, J. Ziegler [1] noted the potential for microelectronics on the ground to be susceptible to SEU from cosmic ray secondaries, primarily neutrons. Ziegler’s work was prompted by the work of T. May and M. Woods [2] in uncovering errors in RAM chips due to upsets caused by the alpha particles released by U and Th contaminants within the chip packaging material. The alpha problem was regarded seriously and chip vendors took specific actions to reduce it to tolerable levels, mainly by reducing the alpha particle flux emitted by packaging and processing materials to generally <0.01 /cm²-hr [3].

Unfortunately, the potential for cosmic rays causing SEU on the ground received little attention, and has received almost no public recognition on the part of chip vendors. Very recently, IBM revealed that beginning in 1979, they undertook a very large proprietary effort to understand the phenomenon of upsets at ground level. This 15-year effort involved many different disciplines and activities: field testing of memories, accelerated testing using cyclotron beams, detailed model development on all levels, environmental monitoring and coordination with device designers [4]. In contrast to the lack of recognition of the key role played by cosmic radiation for ground level upsets, the importance of this mechanism was recognized by people dealing with avionics, i.e., electronics in aircraft, relatively early in the open literature. Avionics SEU by the atmospheric neutrons was first predicted in 1984 [5] and later rigorously demonstrated to occur in flight in 1992[6].

Varios

**DEFINICION**

Single Event Effects (SEE) are caused by one single incoming particle. As an example, in space outside the atmosphere there is a flux of cosmic rays, i.e., protons, ( particles and atomic nuclei at high energies. If just one such charged particle happens to hit the active volume in a bit of a computer memory, it deposits free charge in it. Since charge is what represents the information (0 = no charge, 1 = more than a minimum amount of charge), this can flip a bit from 0 to 1 (or vice versa). Thus, nature is randomly re-programming computer memories due to the action of cosmic rays.  
 

The atmosphere provides very efficient shielding from these cosmic rays, but still there are problems also at ground level. The primary cosmic rays (mostly protons) induce nuclear reactions in the upper atmosphere, so called spallation reactions. This essentially means that a high-energy proton hits a nitrogen or oxygen atomic nucleus and smashes it into pieces. The result of this is a whole spectrum of various particles with a wide range of energies. Most of these particles are stopped by the atmosphere, but some of them penetrate it and reach altitudes occupied by man (0-10 km). The most important particles for SEE are neutrons, which are uncharged and therefore penetrate the atmosphere rather efficiently, and they interact strongly with nuclei, which makes them efficient in causing SEEs.  


Another source of SEEs are impurities in the device material. For instance, in lead used for soldering, there might be traces of uranium or thorium, which both are naturally radioactive elements, decaying by α emission. The α particle can then release charge and cause a SEE.

**There is a formal technical definition of SEE:**

“SEE is any measurable or observable change in state or performance of a microelectronic device, component, subsystem, or system (digital or analog) resulting from a single energetic particle strike. SEE include single-event upset (SEU), multiple-bit upset (MBU), multiple-cell upset (MCU), single-event functional interrupt (SEFI), single-event latch-up (SEL), single-event hard error (SHE),single-event transient (SET), single-event burnout (SEB), and single-event gate rupture (SEGR).”

(JEDEC Standard JESD 89A, ”Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices”, 2006)

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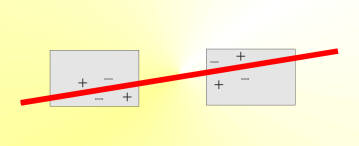
A *single event effect* (SEE) results from, as the term suggests, a single, energetic particle. The possibility of single-event upsets was first postulated by Wallmark and Marcus in 1962.[1] The first actual satellite anomalies were reported by Binder *et al.* in 1975.[2] Some of the early pioneering work was by May and Woods, who investigated alpha-particle-induced soft errors.[3] In their work the source of alpha particles was not from space but rather from the natural decay of trace (ppm) concentrations of uranium and thorium present in integrated circuit packaging materials.

Single event phenomena can be classified into three effects (in order of permanency):

1. Single event upset (soft error)
2. Single event latchup (soft or hard error)
3. Single event burnout (hard failure)

**Single Event Upset**

*Single event upset* (SEU) is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." [Ref: NASA Thesaurus] SEUs are transient soft errors, and are non-destructive. A reset or rewriting of the device results in normal device behavior thereafter. An SEU may occur in analog, digital, or optical components, or may have effects in surrounding interface circuitry. SEUs typically appear as transient pluses in logic or support circuitry, or as bit flips in memory cells or registers. Also possible is a *multiple-bit SEU* in which a single ion hits two or more bits causing simultaneous errors. Multiple-bit SEU is a problem for single-bit *error detection and correction* (EDAC) where it is impossible to assign bits within a word to different chips (*e.g.*, a problem for DRAMs and certain SRAMs). A severe SEU is the single-event functional interrupt (SEFI) in which an SEU in the device's control circuitry places the device into a test mode, halt, or undefined state. The SEFI halts normal operations, and requires a power reset to recover.

  
[Source: [Space Radiation Associates](http://www.spacerad.com/)]

**Single Event Latchup**

*Single event latchup* (SEL) is a condition that causes loss of device functionality due to a single-event induced current state. Kolasinski *et al.* first observed SEL in 1979 during ground testing.[4] SELs are hard errors, and are potentially destructive (*i.e.*, may cause permanent damage). The SEL results in a high operating current, above device specifications. The latched condition can destroy the device, drag down the bus voltage, or damage the power supply. Originally, the concern was latchup caused by heavy ions, however, latchup can be caused by protons in very sensitive devices.[5,6] An SEL is cleared by a power off-on reset or power strobing of the device. If power is not removed quickly, catastrophic failure may occur due to excessive heating, or metallization or bond wire failure. SEL is strongly temperature dependent: the threshold for latchup decreases at high temperature, and the cross section increases as well.[7,8]

**Single Event Burnout**

*Single event burnout* (SEB) is a condition that can cause device destruction due to a high current state in a power transistor. SEB causes the device to fail permanently. SEBs include burnout of power MOSFETs, gate rupture, frozen bits, and noise in CCDs (charge-coupled devices). SEB of power MOSFETs was first reported by Waskiewicz *et al.* in 1986.[9] Only SEB of n-channel power MOSFETs has been reported.[10] An SEB can be triggered in a power MOSFET biased in the OFF state (*i.e.*, blocking a high drain-source voltage) when a heavy ion passing through deposits enough charge to turn the device on. SEB susceptibility has been shown to decrease with increasing temperature.[11]

A power MOSFET may undergo *single-event gate rupture* (SEGR), which is the formation of a conducting path (*i.e.*, localized dielectric breakdown) in the gate oxide resulting in a destructive burnout. Fischer was the first to report on SEGR of power MOSFETs in 1987.[12] SEB can also occur in bipolar junction transistors (BJTs) as was first reported by Titus *et al.* in 1991.[13] Swift *et al.* have described a new hard error, that of single-event dielectric rupture (SEDR).[14] SEDR (also referred to as micro-damage) occurs in CMOS and is similar to SEGR observed in power MOSFETs.

## Environmental and Design Factors

To estimate the upset rate, one must consider the mechanism by which radiation particles cause the anomaly. The SEUs are caused by two different space radiation sources:

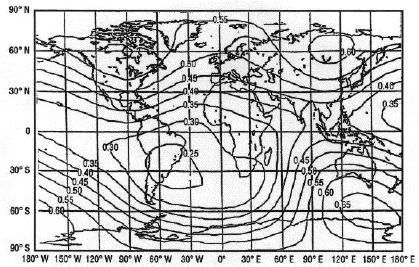
1. high energy protons, and
2. cosmic rays, specifically, the heavy ion component of either solar or galactic origins.

The latter heavy ions cause direct ionization within a device. Protons can make a large contribution to the overall upset rate (particularly for LEO). When the feature size is <0.3 µm, then protons will create SEU by direct ionization. Protons typically do not cause an upset through direct ionization, but rather through complex nuclear reactions (spallation) in the vicinity of the sensitive node (see figure below). *Spallation* is a nuclear reaction in which two or more fragments or particles are ejected from the target nucleus; it is the heavy recoil nuclei ions, such as 25Mg, which can then cause SEU. Example spallation reactions from neutrons and protons include Si(*n*,a)Mg, Si(*n*,*p*)Al [15], Si(*p*,2*p*)Al, and Si(*p*,*p*a)Mg.[16,17,18]

  
Schematic showing how galactic cosmic rays deposit energy in an electronic device.  
(Source *Spacecraft Anomalies due to Radiation Environment in Space* by Lauriente and Vampola [19])

Solar flare particle events pose the most extreme SEU producing environment, especially for spacecraft in interplanetary space.[20] Experiments aboard the Combined Release and Radiation Effects Satellite (CRRES) showed a dramatic increase during a solar flare.[21] However, 90% of all SEUs on CRRES were produced by protons contrary to the pre-launch prediction that most upsets would be caused by cosmic rays.[22] Gussenhoven *et al.* state that based on CRRES data that most single-event upsets come from high energy protons via nuclear interactions and not through direct deposition from either protons or cosmic rays.[23] For LEO satellites, trapped protons, especially in the South Atlantic Anomaly (SAA), are the greatest SEE threat. The SAA, located at 30° S. latitude, 34.5° E. longitude, is shown in the geomagnetic field of Figure 2. Solar cycle activity affects the presence of trapped electrons and protons as shown below:

|  |  |  |
| --- | --- | --- |
|  | Solar Min | Solar Max |
| Electron Intensities | lower | higher |
| Proton Intensities | higher | lower |

  
Geomagnetic field at sea level. Note the South Atlantic Anomaly (SAA) which is centered off the southeastern coast of South America  
(from the [Space Environments & Effects Program](http://see.msfc.nasa.gov/) at NASA's Marshall Space Flight Center).

Given the division of SEEs into soft and hard errors, it is obvious that permanent hard errors are to be completely avoided. Avoidance may be realized through parts selection and shielding. Unfortunately, shielding is of little value for preventing SEUs. For mitigating soft SEEs, other methods, such as error detection and correction (EDAC), and redundancy, may be employed.

Shielding typically has little effect. Shielding high-energy protons while observing weight restrictions is a difficult task. Adams found that under some conditions that shielding can worsen the problem, since as ions slow down in the shielding their LET increases.[24] Shielding produces significant reductions in soft components like solar flare particles, and moderate reductions in the trapped proton flux. Shielding is ineffective against galactic cosmic rays due to their high energies.

#### Critical Charge

SEU was first observed in bipolar flip-flops in 1979. Original work in this area was treated with skepticism. SEU has emerged as one of the major issues for application of microelectronics in space. SEU effects have become worse as devices have evolved because of lower “critical charge” due to small device dimensions, and large numbers of transistors per chip and overall complexity. Nichols ranks the susceptibility of current technologies to SEUs:[25]

* CMOS/SOS (least susceptible)
* CMOS
* Standard bipolar
* Low power Schottky bipolar
* NMOS DRAMs (most susceptible)

For GaAs circuits, latchup and burnout do not occur.[26] However, SEU susceptibility is slightly higher in GaAs devices than in Si devices.[27]

Device immunity is determined by its *linear energy transfer threshold* (LETth). The LETth is defined as the minimum LET to cause a single-event effect at a particle fluence of 107 ions/cm2. SEE-immune is defined as a device having an LETth > 100 MeV·cm²/mg [28] (~iron threshold, Z>26). Low LETth implies proton sensitivity. If a device is not SEU immune, the device is analyzed for SEU rates and effects as follows:

|  |  |
| --- | --- |
| **Device LETth** | **Environment to be Assessed** |
| < 10 MeV·cm²/mg | Cosmic ray ions, trapped protons, solar flare protons |
| 10 - 100 MeV·cm²/mg | Cosmic ray ions |
| > 100 MeV·cm²/mg | No analysis required |

The LETth usually reduces as a device accumulates large TID.[29]

The present trends (*e.g.*, device size and power reduction, line resolution increase, increased memory and speed) will only heighten the SEU susceptibility. This is easily seen when one considers the device as a simple capacitor (*C*) upon which the ionized particle deposits sufficient charge (*Q*) to result in a voltage (*i.e.*, logic state) change. SEU occurs when LET > *Qcrit*.

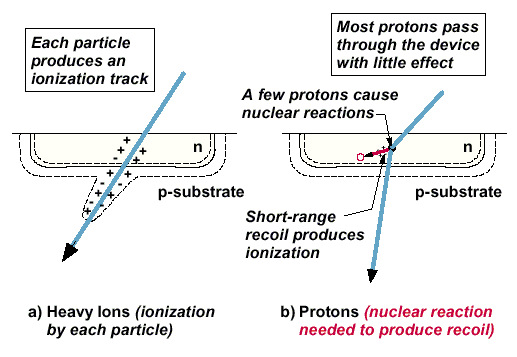
Since the LETth is equivalent to the LET required to produce a voltage change (D*V*) sufficient for an SEU, then mathematically:

LETth a D*V* = *Q*/*C*

As the size of these active devices decreases, the capacitance will decrease and so the charge necessary to induce the SEU. The depth of the devices has been generally unchanged; it is the length and width of these devices that have been reduced. If we consider a square device of feature size, *L x L*, the critical charge for state change is proportional to the feature size squared (*Qcrit* a *L*2). Robinson *et al.* present the measured critical charge for a number of IC technologies (including NMOS, CMOS/bulk CMOS/SOS, i2L, GaAs, ECL, CMOS/SOI, and VHSIC bipolar) as being:[30]

*Qcrit* = (0.023 pC/µm2) *L*2

This *critical charge* is that charge necessary to flip a binary "1" to a "0" or vice-versa, but is less than the total stored charge. Specifically, *Qcrit* is then the difference between the storage node charge and the minimum charge required for the sensing amplifier to read correctly.[31] In SRAM circuits, *Qcrit* depends not just on the charge collected but also the temporal shape of the current pulse.

  
[Source: "[Space Radiation Effects on Microelectronics](http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf)," NASA Jet Propulsion Laboratory]

**Elementary Model for Heavy Ions**

A very elementary model of SEU behavior can be formed using the concept of LET through some depth of a parallelepiped-shaped device. Start by calculating the energy deposited, *Edep*, as the particle traverses a chord of length *s* through the sensitive volume of the device (see diagram below).

*Edep* = *LET* p *s*

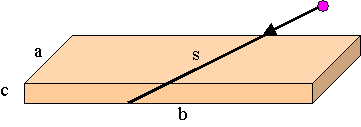
The deposited charge depends on the energy required to generate an electron-hole pair, *wehp*,

*Qdep* = *Edep q* / *wehp*

where *q*=1.6022x10-19 Coulombs/*e* and *wehp* for a few materials are given in the table below:

Properties of intrinsic germanium, silicon, gallium arsenide, silicon dioxide, silicon nitride, and aluminum oxide at 27°C unless otherwise noted.[27]

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Material** | **Ge** | **Si** | **GaAs** | **SiO2** | **Si3N4** | **Al2O3** |
| Type | Semiconductor | Semiconductor | Semiconductor | Insulator | Insulator | Insulator |
| Atomic/Molecular Weight | 72.6 | 28.09 | 144.63 | 60.08 | 140.27 | 101.96 |
| Density (g/cm3) | 5.33 | 2.33 | 5.32 | 2.27 | 3.44 | 3.97 |
| Electron-hole pair generation energy (eV) | 2.8 | 3.6 | 4.8 | 17. | 10.8 | 19.1 |



Using such a simple approach, a first-order estimate of the minimum LET required for causing an SEU can be computed. Consider a parallelepiped of dimensions *a*, *b*, *c* where *c* is the device depth. The minimum LET corresponds to the maximum chord length possible, *smax*, which is the diagonal of the parallelepiped.

*s2max* = *a*2 + *b*2 + *c*2

The minimum LET necessary to cause an upset can then be calculated from

LETth = *Qcrit wehp* / (*q* p *smax*)

Likewise, there is a minimum distance, *smin*, that a particle of given LET must travel before being able to deposit sufficient energy to cause an SEU.

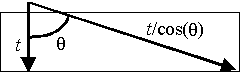
*smin* = *Qcrit wehp* / (*q* p LET)

Hence, the particle *angle of incidence* upon the device is also important. As the incidence angle deviates from normal, the path length traversed by the radiation increases. The angle from incident at which upsets occur for a given particle LET is known as the *critical angle*, Oc

cos(Oc) = LET / LETC

The particles that produce upset are between an angle of Oc and pi/2. Therefore, there are two potential cases (note LETC < LETth)

1. If LET > LETC, then all incident angles produce upset.
2. If LET < LETC, then there is a critical angle, Oc, above which upsets occur.

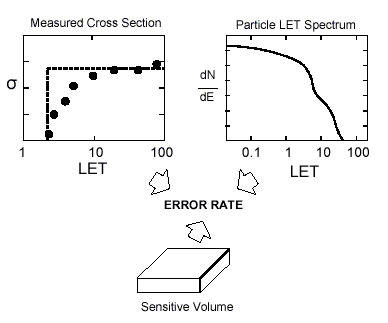


For a parallelepiped particles incident at an angle O have a path that is 1/cos(O) longer than the path at normal incidence, thus producing more ionization charge. [Note: This "cosine law" fails in some cases, and must be checked for each device technology.] Unlike SEU behavior, SEB and SEGR susceptibility has been shown to decrease with increasing angles of incidence. [7,8,32,33]

The energy deposited per unit path length as an energetic particle travels through a material is the *linear energy transfer* (LET). Note that the LET is normally defined by *dE*/*dx*; however, the LET used in SEU studies is actually the *mass stopping power* defined by (*dE*/*dx*)/p where p is the material density. This results in an LET unit of MeV/(mg/cm2) of material, which is the energy loss per density thickness. *Density thickness* (*td*) is the product of the material density and its thickness (*t*), *i.e.*, *td* =p·*t*. Therefore, the density thickness describes the areal density of electrons (electrons/cm2). The LET is dependent on the particle, its energy, and the material traversed.

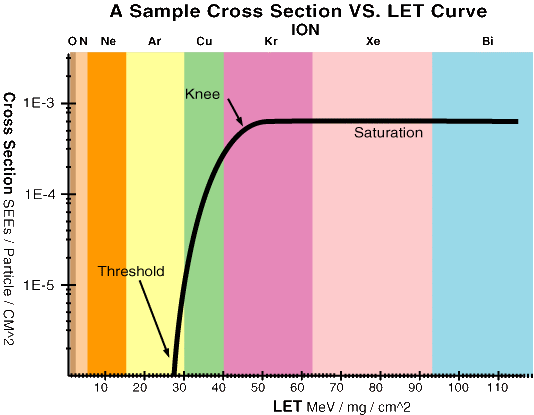
**Practical SEU Calculation**

The upset rate may be reported as errors per day per chip, or errors per day per bit (errors/bit-day). Error rates of hardened devices can be of the order of 10-8 errors/bit-day; unhardened devices are generally several orders of magnitude higher.

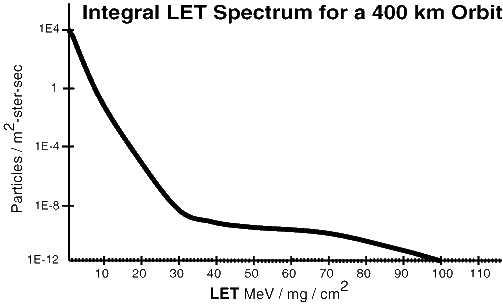
  
[Source: "[Space Radiation Effects on Microelectronics](http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf)," NASA Jet Propulsion Laboratory]

There are three basic steps in the calculation of SEU Rates:

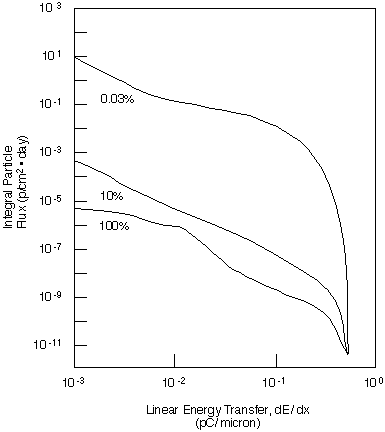
1. Measure the cross section (s) versus LET for example using accelerator testing. The device *cross section* is defined as the ratio of the number of upsets to the particle fluence. The experimentally determined cross section is a function of particle energy (LET).

  
[Source: The Aerospace Corporation [SEE Primer](http://www.aero.org/capabilities/seet/primer.html)]

1. Determine the sensitive device volume. The sensitive volume is smaller than the actual device physical volume. The sensitive volume is generally different for SEE from heavy ions and protons, as well as SEL. The sensitive geometry and critical charge are the most difficult parameters to determine.
2. To determine the device error rate, integrate the cross section and sensitive device volume with the LET spectrum.

  
[Source: The Aerospace Corporation [SEE Primer](http://www.aero.org/capabilities/seet/primer.html)]

In LEO, the inner belt (trapped) protons are the most important source. For LEO satellites, trapped protons, especially in the South Atlantic Anomaly (SAA), are the greatest SEE threat. For GEO, the cosmic and solar particles initiate SEEs. The galactic cosmic ray environment is modeled using CREME; the solar flares can be modeled using JPL or CREME models. Solar flare particle events pose the most extreme SEU producing environment, especially for spacecraft in interplanetary space.[20]

  
[Source: [The NASA ASIC Guide: Assuring ASICS for Space](http://parts.jpl.nasa.gov/asic/title.page.html)]

The Heinrich Curve above shows the integral energy loss spectrum at GEO. The 100% curve corresponds to solar max condition, and the environment is always worse. The 10% curve combines solar minimum cosmic rays and solar proton activity so that the environment is worse only 10% of the time. The 0.03% curve corresponds to an anomalously large solar flare.

Petersen *et al.* have developed a simple expression for the upset rate at GEO from galactic rays.[34] The GEO flux is due to galactic cosmic rays since protons at the outer edge of the radiation belts is assumed negligible. SEU error rate expressions are obtained using chord distribution function for the cross section. After integrating the flux and cross section over the range of energies (LET), the "figure of merit" formula for the error rate for the 10% environment results:

*R* = 5x10-10 ssat / (LETcrit)2

where *R* is the SEU error rate in errors per bit-day; ssat is the saturation SEU cross section in µm2; and LETcrit is the critical LET in units of pC/µm. For design purposes, the error rate may be estimated using the above expression with ssat = *a b* with (*a*,*b* >> *c*), and LETcrit=*Qcrit*/*c* where *c* is the silicon device depth, and *a*and *b* are its sides in microns (µm). The above expression provides an upper-bound estimate. One can replace the numeral 5 in the “figure of merit” equation with a value of 3.5 for GaAs devices. Multipliers have been developed for the figure of merit (FOM) formula to scale the error rate to other environments, especially solar flares:

|  |  |
| --- | --- |
| **Environment** | **Multiplier** |
| Petersen model (SEU figure of merit) | 1.0 |
| Galactic model (solar minimum) | 0.44 |
| "Ordinary" flare | 13 |
| 90% worst-case flare | 33 |
| Anomalously large flare | 5000 |